Remarks

Reconsideration of the application is respectfully requested in view of the foregoing amendments and following remarks. Claims 1-5 and 35-46 are pending in the application. No claims have been allowed. Claims 1 and 40 are independent.

Response to § 103(a) Rejections

The Action rejects claims 1-5 and 35-46 under 35 U.S.C. § 103(a). Applicants respectfully traverse these rejections.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. In addition, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (*See* MPEP § 2142.) Motivations to combine or modify references must come from the references themselves or be within the body of knowledge in the art. (*See* MPEP § 2143.01.)

Applicants respectfully submit that the claims in their present form are allowable over the applied art, as explained in detail below.

A. Response to Rejection of Claims 1-3, 5, 35, 39-41, 45 and 46

In the Action, the Office rejects claims 1-3, 5, 35, 39-41, 45 and 46 under § 103(a) in view of U.S. Patent Application Publication No. 2004/0190771 ("Eid"), U.S. Patent Application Publication No. 2001/0025292 ("Denk"), and Motorola, Inc., *M68000 8-/16-/32-Bit Microprocessors Programmer's Reference Manual*, p. B-35 (5th ed. 1986) ("Motorola"). Applicants respectfully traverse these rejections.

As amended, independent claim 1 recites in part:

> the n-bit representation comprising a 16-bit fixed-point block of data per channel for the pixel, where the most significant byte in the 16-bit unit of data is an integer component, where the least significant byte in the 16-bit unit of data is a fractional component, and where *the n-bit representation is convertible to a lower-precision representation by assigning zero values to one or more least significant bits in the fractional component while the integer component is unchanged.*

[Emphasis added.]

Independent claim 40 recites in part:

> the n-bit representation comprising a 16-bit fixed-point block of data per channel for the pixel, where the most significant byte in the 16-bit unit of data is an integer component, where the least significant byte in the 16-bit unit of data is a fractional component, and where *the n-bit representation is convertible to a lower-precision representation by assigning zero values to one or more least significant bits in the fractional component while the integer component is unchanged.*

[Emphasis added.]

Eid, Denk and Motorola, individually or in combination, do not teach or suggest the above-cited language of independent claims 1 and 40. In particular, Eid, Denk and Motorola do not teach or suggest "the n-bit representation is convertible to a lower-precision representation by assigning zero values to one or more least significant bits in the fractional component while the integer component is unchanged," as recited in independent claims 1 and 40.

The Action states at pages 3-4,

> The combination of Eid and Denk discloses shifting and rounding operations, but they do not explicitly teach to assign zero values to one or more of the bits in the least significant byte while the most significant byte is unchanged. However, Motorola's M68000 Programmer's Reference Manual teaches to use CLR command to clear the destination to all zero (page B-35; using CLR command, the least significant byte of the higher precision representation could be assigned zero values and converted to the lower precision representation). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the present invention to assign zero values to the least significant byte of the higher precision representation as taught by Motorola . . . .

Applicants agree that the combination of Eid and Denk does not teach or suggest the above-cited language of independent claims 1 and 40. However, Applicants respectfully disagree that Motorola teaches or suggests "to assign zero values to the least significant byte of the higher precision representation" as stated by the Examiner. Motorola is even further from teaching or suggesting "assigning zero values to one or more least significant bits in the fractional component while the integer component is unchanged," as recited in independent claims 1 and 40.

Motorola describes an operation named "0 → Destination" in which "[t]he destination is cleared to all zero." The instruction format for the "0 → Destination" operation includes an "Effective Address" field that "[s]pecifies the destination location" in memory and a "Size" field that "[s]pecifies the size of the operation" to clear memory of size byte, word, or long. [*See id.*]

Although Motorola describes clearing a "destination" to zero, the cited operation in Motorola

does not teach or suggest an n-bit representation that is *convertible to a lower-precision representation by assigning zero values. In particular, Motorola does not assign zero values to bits in a fractional component of a destination or any other data.* The description of the "0 → Destination" operation does not describe a fraction or integer component for a destination location or for whatever might be in memory at the destination location. [*See id.*] Clearing a memory location to zero as described by Motorola does not convert anything to a lower-precision representation. In fact, page B-35 of Motorola teaches directly away from reducing precision of data because a memory location specified in the instruction is *completely cleared to zero*, effectively erasing whatever data was there. [*See id.*] A combination of Motorola with Eid and Denk would actually lead to clearing memory of data described in Eid and Denk, rather than leading to the above-cited language of claims 1 and 40.

Claims 1 and 40 are allowable. Claims 2, 3, 5, 35 and 39 depend from claim 1 and are allowable for at least the reasons given above in support of claim 1. Claims 41, 45 and 46 depend from claim 40 and are allowable for at least the reasons given above in support of claim 40. Therefore, the rejection of claims 1-3, 5, 35, 39-41, 45 and 46 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Dependent claims 4, 36-38 and 42-44 also are allowable. The rejections of dependent claims 4, 36-38 and 42-44 are addressed below.

B. Response to Rejection of Claim 4

In the Action, the Office rejects claim 4 under § 103(a) in view of Eid, Denk, Motorola and U.S. Patent Application Publication No. 2004/0183949 (Lundberg et al.). Applicants respectfully traverse this rejection.

The applied art does not teach or suggest each and every element of dependent claim 4. Lundberg describes "the colour information in each picture is sampled at lower spatial resolution than the luminance." [See Lundberg at ¶ 0073.] However, the applied art does not teach or suggest the recited language of independent claim 1, from which claim 4 depends. For example, Lundberg does not teach or suggest "the n-bit representation is convertible to a lower-precision representation by assigning zero values to one or more least significant bits in the fractional component while the integer component is unchanged," as recited in independent claim 1.

Because the applied art does not teach or suggest at least one element of independent claim 1, claim 4 is allowable for at least the reasons given above for the allowability of its parent claim. Therefore, the rejection of claim 4 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

C. **Response to Rejection of Claims 38 and 44**

In the Action, the Office rejects claims 38 and 44 under § 103(a) in view of Eid and "FOURCC.org – YUV pixel formats," http://www.fourcc.org/yuv.php, pp. 1-15 ("the FOURCC.org YUV pixel formats document"). Applicants respectfully traverse this rejection.

The applied art does not teach or suggest each and every element of dependent claims 38 and 44. The FOURCC.org YUV pixel formats document describes packed YUV formats with different numbers of bits per pixel, but the applied art does not teach or suggest the recited language of independent claims 1, from which claim 38 depends, or independent claim 40, from which claim 44 depends. For example, the FOURCC.org YUV pixel formats document does not teach or suggest "the n-bit representation is convertible to a lower-precision representation by assigning zero values to one or more least significant bits in the fractional component while the integer component is unchanged," as recited in independent claims 1 and 40. In addition, the web page at http://www.fourcc.org/yuv.php cited by Applicants in the IDS filed on March 10, 2004, indicates a "last modified" date of February 7, 2004. Applicants do not admit that this document is prior art to the present application and reserve the right to provide evidence of prior conception.

Claims 38 and 44 are allowable for at least the reasons given above for the allowability of their respective parent claims. Therefore, the rejection of claims 38 and 44 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

D. **Response to Rejection of Claims 36, 37, 42 and 43**

In the Action, the Office rejects claims 36, 37, 42 and 43 under § 103(a) in view of Eid and U.S. Patent Application Publication No. 2003/0202589 (Reitmeier et al.). Applicants respectfully traverse this rejection.

The applied art does not teach or suggest each and every element of dependent claims 36, 37, 42 and 43. Reitmeier describes a "10-bit video signal is coupled to a video processor (not shown) for

further processing." [See Reitmeier at ¶ 0033.] However, the applied art does not teach or suggest the recited language of independent claim 1, from which claims 36 and 37 depend, or independent claim 40, from which claims 42 and 43 depend. For example, Reitmeier does not teach or suggest "the n-bit representation is convertible to a lower-precision representation by assigning zero values to one or more least significant bits in the fractional component while the integer component is unchanged," as recited in independent claims 1 and 40.

Claims 36, 37, 42 and 43 are allowable for at least the reasons given above for the allowability of their respective parent claims. Therefore, the rejection of claims 36, 37, 42 and 43 under 35 U.S.C. § 103(a) should be withdrawn. Such action is respectfully requested.

Request For Interview

If any issues remain, the Examiner is formally requested to contact the undersigned attorney prior to issuance of the next Office Action in order to arrange a telephonic interview. It is believed that a brief discussion of the merits of the present application may expedite prosecution. Applicants submit the foregoing formal Amendment so that the Examiner may fully evaluate Applicants' position, thereby enabling the interview to be more focused.

This request is being submitted under MPEP § 713.01, which indicates that an interview may be arranged in advance by a written request.

Conclusion

The claims in their present form should now be allowable. Such action is respectfully requested.

Respectfully submitted,

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